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MemorES3: a programmable, real-time hardware **emulation** tool for multiprocessor server ...

A Nanda, KK Mak, K Sugaryanam, RK Sahoo, ... - Proceedings of the ninth international conference on ..., 2000 - portal.acm.org

... The four cache **emulation** **FPGAs** are designed to always run in **lock step** mode regardless of the cache parameter settings. This simplifies ...

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System and a method for checking **lock step** consistency between an in circuit **emulation** and ...

C Nemecek - US Patent 6,922,821, 2005 - Google Patents

... Thus, design and realization of the **FPGA** implementation of an **emulator** for the ... Thus, the **FPGA**, by virtue of operating in **lock-step** operation with the ...

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Host to **FPGA** interface in an in-circuit **emulation** system

C Nemecek - US Patent 7,206,733, 2007 - Google Patents

... 10, 2001; US Time Debugging Using **FPGA** for In-Circuit **Emulation**"; Oct. 10, Appl. No. 09/975,338; Nemecek et al. 2001; US Appl. No. 09/975,104; Snyder. ...

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... test/**emulation** and enabling real-time debugging using an **FPGA** for in-circuit **emulation**

W Snyder - US Patent 7,188,063, 2007 - Google Patents

... The two devices, the micro- 20 In-Circuit **Emulation** system consistent ... Present Invention viewed from a virtual microcon- **lock-step** with the **FPGA** acting as ...

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Emulator chip/board architecture and interface

W Snyder, C Nemecek, B Sullam - US Patent 7,076,420, 2006 - Google Patents

... The bus allows the **FPGA** and microcontroller to ... with an **emulator** device, the **emulator** device implementing ... DUT and executing instructions in **lock-step** with the ...

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In-circuit **emulator** with gatekeeper for watchdog timer

C Nemecek, S Roe - US Patent 7,162,410, 2007 - Google Patents

... block diagram isolating the host to **FPGA** having a ... of the present running in **lock-step** synchronization with ... A host computer runs In-Circuit **Emulation** debug soft ...

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An **FPGA**-based Pentium® in a complete desktop system - ► [toronto.edu](#) [PDF]

SLL Lu, P Yiannacouras, R Kassa, M Konow, ... - Proceedings of the 2007 ACM/SIGDA 15th ..., 2007 - portal.acm.org

... 1: Image of the **FPGA**-based processor **emulator** system equipped ... 3.4 **FPGA** Development

To synthesize the Pentium r we ... used to simulate the VHDL in **lockstep** with a ...

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Combined in-circuit **emulator** and programmer

C Nemecek, S Roe - US Patent 7,089,175, 2006 - Google Patents

... FIG 6 is a block diagram isolating the host to **FPGA** A combined in-circuit **emulation** system and programmer interface consistent with an embodiment of the ...

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In-circuit **emulator** with gatekeeper based halt control

C Nemecek, S Roe - US Patent 7,236,921, 2007 - Google Patents

... for an In-Circuit **Emulation** sys- tem ... a virtual microcontroller that operates in **lock-step** synchronization with ... 1-30.* Bursky, "FPGA Combines Multiple Interfaces ...[All 2 versions](#)System and a method for communication between an ICE and a production microcontroller ...

C Nemecek - US Patent 6,957,180, 2005 - Google Patents

... 3 US 6,957,180 BI RUN CODE IN **LOCKSTEP** - ICE KEEPS ... The base station 218's **FPGA** based virtual microcontrol- ler 220 ... execution of the code is in **lock step** and it ...[Cited by 1](#) - [Related articles](#) - [All 2 versions](#)

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